Customer No.: 31561
Docket No.: 13041-US-PA
Application No.: 10/710,732

Amendments

In the Specification:

Please amend the specification as follows:

[0025] Figs. 4 through 9 are schematic cross-sectional views showing the steps of fabricating a photodiode according to the present invention. First, as shown in Fig. 4, a substrate 400 is provided. The substrate 400 can be a P-type or an N-type silicon substrate, for example. Thereafter, a well region 402 of a first conductive type is formed in the substrate 400. The well region 402 is formed, for example, by forming a mask layer (not shown) over the substrate 400 to define a region (not shown) of the substrate 400 designated for forming the well region 402 and then performing an ion implantation process to form the well region 402 in the substrate 400. P-type dopants or N-type dopants can be used in the implantation to produce a P-type well or an N-type well 402.

[0026] As shown in Fig. 5, an isolation structure 404 is formed in the well region 402 of the substrate 400 to define a photosensitive area 406. The isolation structure 404 can be a shallow trench isolation (STI) structure or a field oxide layer formed in a local oxidation of silicon (LOCOS) process, for example. The isolation structure 404 mainly serves as a barrier preventing any portion of an induced current from diffusing into neighboring sensing devices or electronic devices to cause mutual interference.

[0027] As shown in Fig. 6, a plurality of trenches such as 408a, 408b, and 408c are formed in the well region 402 of the substrate 400 within the photosensitive area 406. For

example, a patterned mask layer (not shown) is formed over the well region 402 of the substrate 400 to define the locations of the trenches 408a, 408b and 408c. Thereafter, an anisotropic etching operation is carried out using the patterned mask layer as an etching mask to form the trenches 408a, 408b and 408c within the photosensitive area 406. Finally, the mask layer over the photosensitive area 406 is removed.

[0028] As shown in Fig. 7, a buffer layer 410 is formed over the photosensitive area 406 covering the interior sidewalls of the trenches 408a, 408b and 408c as well as the upper surface of the well region 402 of the substrate 400. The buffer layer 410 is formed by polysilicon or epitaxial silicon in a chemical vapor deposition process, for example. It should be noted that the buffer layer 410 is optional. In other words, this particular step of forming the buffer layer 410 can be skipped without any effect on the operation of the photodiode.

[0031] Fig. 10 is a schematic cross-sectional view of a portion of the photodiode fabricated according to the method of the present invention. Components in Fig. 10 identical to the ones in Figs. 4 through 9 are labeled identically. As shown in Fig. 10, one major aspect of the present invention is the etching of the well region 402 of the substrate 400 to form the trenches 408a, 408b and 408c in the well region 402 of the substrate 400. Another aspect of the present invention is the performance of a chemical vapor deposition process to form the buffer layer 410 and the doped layer 412 on the inner walls of the trenches 408a, 408b and 408c as well as a portion of the upper surface of the well region 402 of the substrate 400. It should be noted that the buffer layer 410 and the annealing operation are optional and hence can be selectively

applied. The buffer layer 410 mainly serves as a buffer between the doped layer 412 and the well region 402 in the substrate 400 so that the P-N junction 414 can be positioned within the buffer layer 410 instead of the well region 402. However, even in the absence of the buffer layer 410 so that the doped layer 412 contacts the well region 402 of the substrate 400 directly, a P-N junction having an adjacent depletion region is still produced to provide the photodiode with a means of detecting external illumination.

[0032] As shown in Fig. 10, a logic circuit area 416 is also formed over the substrate 400 outside the isolation structure 404 enclosed photosensitive area 406. Inside the logic circuit area 416, an electronic device such as a reset transistor 418 is disposed. The device within the logic circuit area 416 is formed before etching out the trenches 408a, 408b and 408c in the well region 402 of the substrate 400 or after all the aforementioned steps have been completed, for example. Since a conventional technique of forming the reset transistor 418 or related devices inside the logic circuit area 416 is deployed, detailed description is omitted.

[0033] In Fig. 10, the doped layer 412 is a uniform thick layer over the buffer layer 410. However, the doped layer may completely fill all the trenches. Fig. 11 is a schematic cross-sectional view of a portion of another photodiode fabricated according to the method of the present invention. As shown in Fig. 11, the buffer layer 510 is a uniform layer covering all the interior walls of the trenches 508a, 508b and 508c as well as the surface of the well region 402 of the substrate 500 between the trenches 508a, 508b and 508c. The doped layer 512 covers the buffer layer 510 globally and completely fills the trenches 508a, 508b and 508c.